JMicron Technology Corp.

Chip Specification

JMS578

SuperSpeed USB 3.0 to SATA 6.0Gb/s Bridge Controller
Revision: 1.0.0

Document No.: 578-00004/Issue Date: Jan-13-2015

JMicron Technology Corporation

1F, No. 13, Innovation Road 1, Science-Based Industrial Park,

Hsinchu, Taiwan 300, R.O.C.

Tel: 886-3-5797389

Fax: 886-3-5799566

Website: http://www.jmicron.com

Certificate No.: FM 84262

© JMicron 2014. All rights reserved.

Copying prohibited.

Revision History

Version	Date	Revision Description
1.0.0	2015/01/13	Formal release

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

CONFIDENTIAL

© Copyright JMicron Technology 2015.

All Rights Reserved.

Printed in Taiwan 2015

JMicron and the JMicron Logo are trademarks of JMicron Technology Corporation in Taiwan and/or other countries. Other company, product and service names may be trademarks or service marks of others.

All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use implantation or other life supports application where malfunction may result in injury or death to persons. The information contained in this document does not affect or change JMicron's product specification or warranties. Nothing in this document shall operate as an express or implied license or environments, and is presented as an illustration. The results obtained in other operating environments may vary.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIEDE ON AN "AS IS" BASIS. In no event will JMicron be liable for damages arising directly or indirectly from any use of the information contained in this document.

JMicron Technology Corporation

1F, No.13, Innovation Road 1,

Hsinchu Science Park,

Hsinchu, Taiwan, R.O.C

For more information on JMicron products, please visit the JMicron web site at

http://www.JMicron.com or send email to sales@jmicron.com

© JMicron 2014. All rights reserved. Copying prohibited.

Table of Contents

1. Overviews....6
1.1 FUNCTION OVERVIEW....6
1.1.1 FEATURES....6
1.1.2 BLOCK DIAGRAM....7
1.2 PACKAGE DIMENSION....8
1.2.1 QFN48 6x6mm^2 (JMS578-QGBA0A)....8
1.3 SUPPORT DEVICES....9
1.4 APPLICATION EXAMPLES....9
1.4.1 USB2.0, USB3.0 to SATA Bridge....9
2. Package Pin-Out....10
2.1 QFN48....10
2.2 PIN TYPE DEFINITION....11
2.3 SERIAL ATA INTERFACE....11
2.4 USB3.0 INTERFACE....11
2.5 USB2.0 INTERFACE....12
2.6 CRYSTAL INTERFACE....12
2.7 VOLTAGE REGULATOR....12
2.8 DIGITAL POWER AND SYSTEM CONTROL INTERFACE....13
3. External SPI Flash....15
3.1 EXTERNAL FLASH PROM/EPROM....15
4. Clock & Reset....17
4.1 Crystal input....17
4.2 Reset input....17
5. Electrical Characteristics....18
5.1 Absolute Maximum Rating....18
5.2 Recommended Power Supply Operation Conditions....18
5.3 Recommended External Clock Source Conditions....18
5.4 Power Supply DC Characteristics....19
5.4.1 Power On (No USB Connected)....19
5.4.2 USB2.0 to SATA mode....19
5.4.3 USB3.0 to SATA mode....19
5.5 I/O DC Characteristics....20
5.6 VBus Detector....20
5.7 Switching Power efficiency (VREG_IN)....21
5.8 Internal Linear Regulator....22

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

5.9 Power Ripple 22
5.10 Power-On Sequence 22
6. Internal Switch Regulator 24
6.1 PCB layout guidelines : 24
7. Performance Benchmark 25
7.1 Platform Configuration 25
7.2 HDD List 25
7.3 Test Tool 25
7.4 JMS578 Performance 26
7.4.1 Win 7 26
7.4.2 Win 8.1 27
8. Product Naming 28
QFN48 6X6 mm^2 28

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

1. Overviews

1.1 FUNCTION OVERVIEW

1.1.1 FEATURES

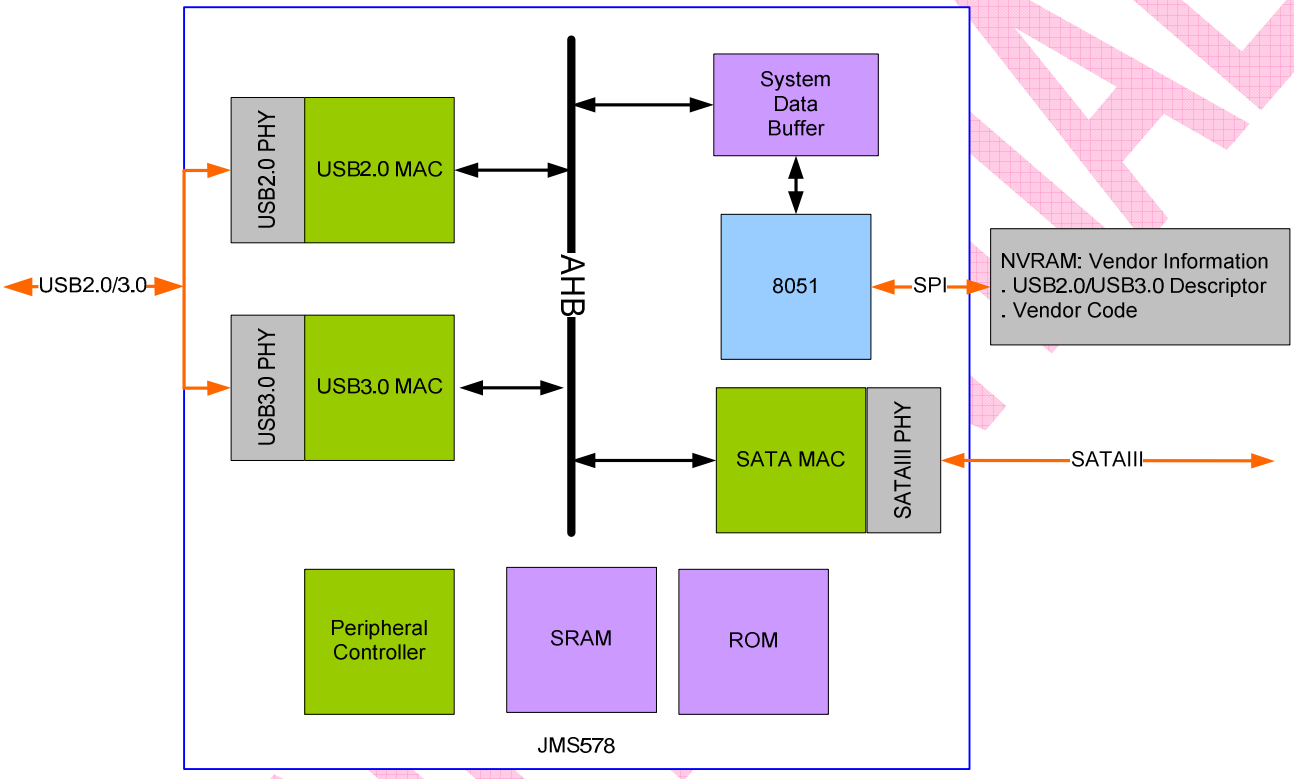
- Complies with Gen2i/Gen2m of Serial ATA II Electrical Specification 2.6
- Complies with Gen3 of Serial ATA III Electrical Specification 3.2
- Complies with USB 3.0 Specification, USB Mass Storage Class, Bulk-Only Transport Specification
- Complies with USB Attached SCSI Protocol (UASP) Specification
- Supports USB Super-Speed/High-Speed/Full-Speed Operation
- Supports USB2.0/USB3.0 power saving mode
- Supports SHA-1/SHA-256 for IEEE-1667 digest calculation
- Supports external SPI NVRAM for Vendor VID/PID of USB2.0/USB3.0 device controller
- Supports ATA/ATAPI PACKET command set
- 10 GPIOs for customization
- Provides hardware control PWM
- Provides software utilities for downloading the upgraded firmware code under USB2.0/USB3.0
- Design for Windows XP, Windows 7, Windows 8.1 and MAC 10.7.4 or later version.
- Supports 30MHz external crystal
- Embedded 5V to 1.2V voltage regulator
- Embedded 5V to 3.3V linear voltage regulator (LDO)
- QFN48 package (6x6)

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

1.1.2 BLOCK DIAGRAM



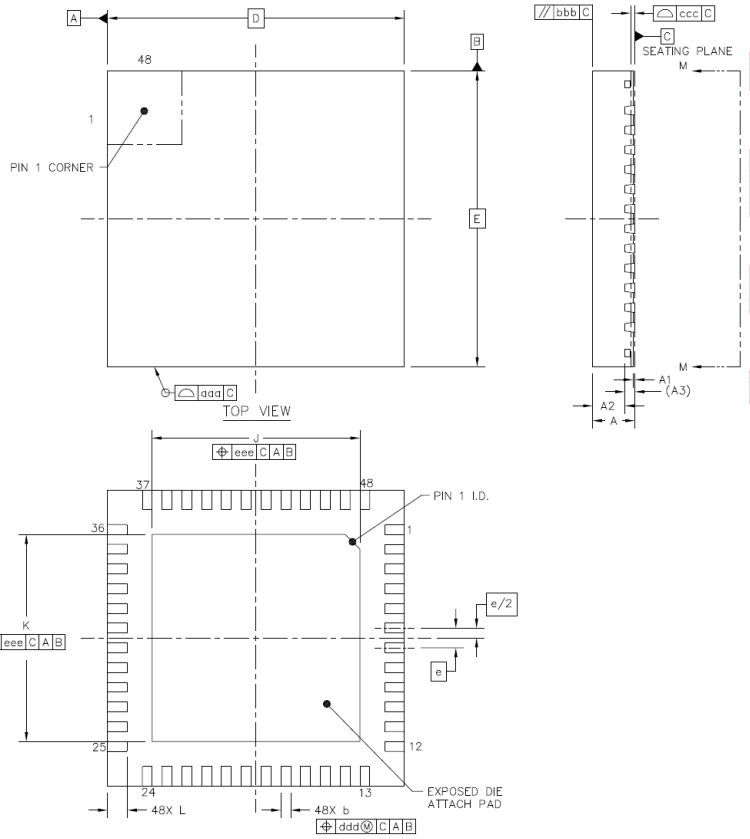
CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

1.2 PACKAGE DIMENSION

1.2.1 QFN48 6x6mm^2 (JMS578-QGBA0A)



Unit: mm

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.1	4.2	4.3
	Y	K	4.1	4.2	4.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Note: The ground pad size is (J * K)

© JMicron 2014. All rights reserved.

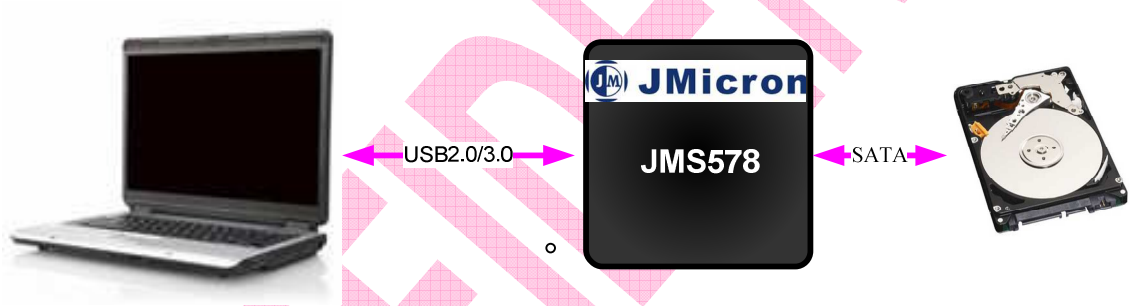
Copying prohibited.

1.3 SUPPORT DEVICES

- Hard disk drivers
- Removable media devices

1.4 APPLICATION EXAMPLES

1.4.1 USB2.0, USB3.0 to SATA Bridge



An example of one SATA application is illustrated.

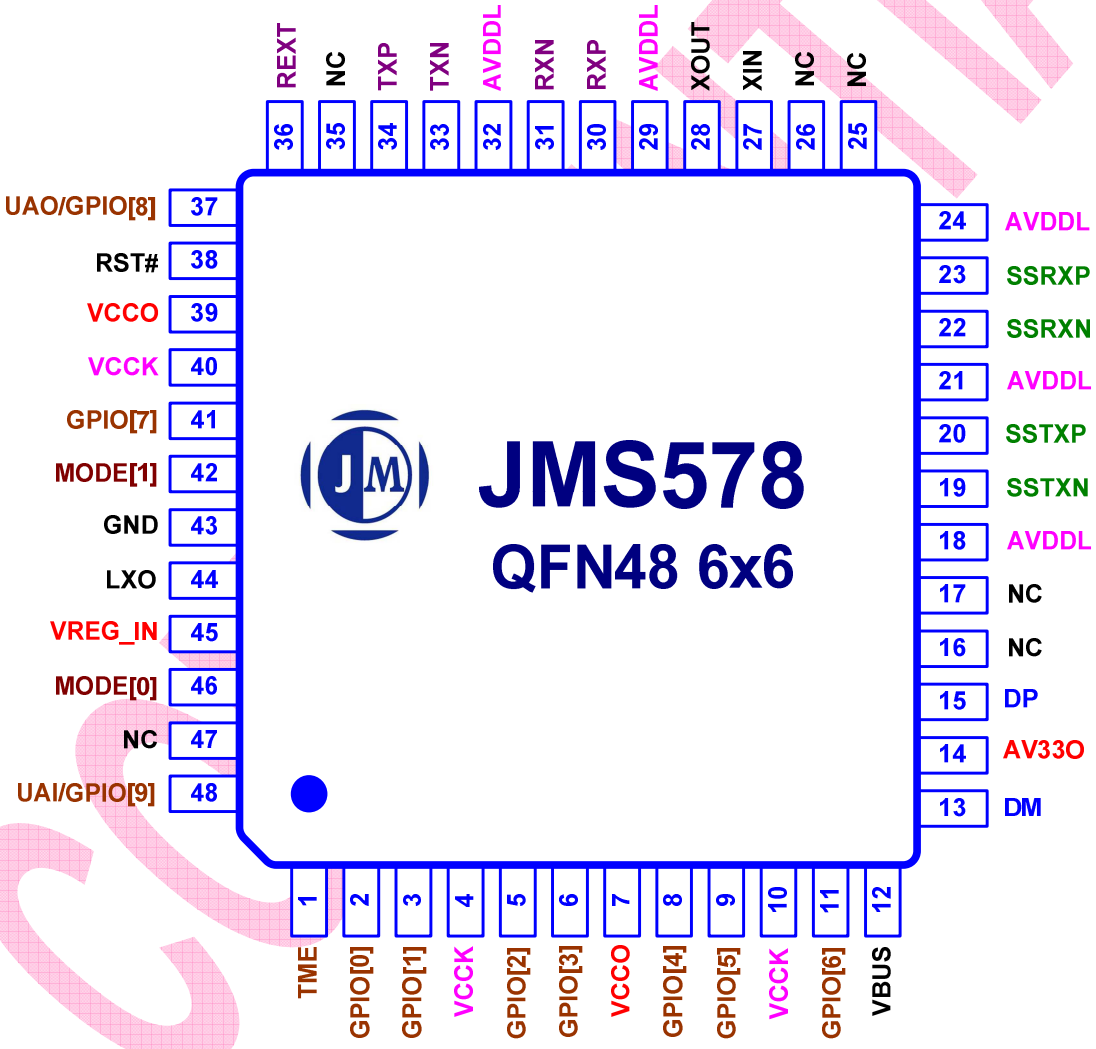
CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

2. Package Pin-Out

2.1 QFN48



© JMicron 2014. All rights reserved.

Copying prohibited.

2.2 PIN TYPE DEFINITION

Pin Type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
L	Internal weak pull-low (Max. 164KΩ, Typical 96 KΩ, Min. 61KΩ)
H	Internal weak pull-high (Max. 141KΩ, Typical 93 KΩ, Min. 66KΩ)

2.3 SERIAL ATA INTERFACE

Signal Name	Pin No.	Type	Description
RXP	30	AI	**Serial ATA Port RX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
RXN	31	AI	**Serial ATA Port RX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXP	34	AO	**Serial ATA Port TX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXN	33	AO	**Serial ATA Port TX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
NC	35	AI	**Non Connect** Don't Care on the connectivity
AVDDL	32	AI	**SATA Analog 1.2V Power Supply.**
REXT	36	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.

2.4 USB3.0 INTERFACE

Signal Name	Pin No.	Type	Description
SSRXP	23	AI	**Super Speed RX+ signal.**
SSRXN	22	AI	**Super Speed RX- signal.**
SSTXP	20	AO	**Super Speed TX+ signal.** A 100nF CAP should be connected between this pin and USB connector.
SSTXN	19	AO	**Super Speed TX- signal.** A 100nF CAP should be connected between this pin and USB connector.

© JMicron 2014. All rights reserved.

Copying prohibited.

Signal Name	Pin No.	Type	Description
NC	16	N/A	**Non Connect** Don't Care on the connectivity
NC	17	N/A	**Non Connect** Don't Care on the connectivity
AVDDL	18,21,24	AI	**USB3.0 Analog 1.2V Power Supply.**

2.5 USB2.0 INTERFACE

Signal Name	Pin No.	Type	Description
DM	13	AIO	**USB2.0 Bus D- Signal.**
DP	15	AIO	**USB2.0 Bus D+ Signal.**
VBUS	12	AI	**USB2.0/3.0 Cable Power Input.**
AV33O	14	AO	**USB2.0 Analog 3.3V Output.** A capacitance to ground is recommended on this pin. The value should be 1uF. The output voltage range is 3.3V±10%. Note: 1. This PIN provides power less than 100mA @ 3.3V. 2. This pin can afford chip internal power usage only.

2.6 CRYSTAL INTERFACE

Signal Name	Pin No.	Type	Description
XIN	27	AI	**Crystal Input/Oscillator Input.** It is connected to a 30MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage should range in 1.2V±5%.
XOUT	28	AO	**Crystal Output.** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved as No Connection (NC). The output variation range is around ±30ppm (input dependent). And the output voltage range is 1.2V±5% (input dependent).
NC	25	N/A	**Non Connect** Don't Care on the connectivity
AVDDL	29	AI	**1.2V Analog Power Supply**

2.7 VOLTAGE REGULATOR

Signal Name	Pin No.	Type	Description
VREG_IN	45	AI	**Voltage Regulator Power Supply**
GND	43	AI	**Voltage Regulator Ground**

© JMicron 2014. All rights reserved.

Copying prohibited.

Signal Name	Pin No.	Type	Description
LXO	44	AO	**Voltage Regulator Output** Switch node. Connect with external power inductor with a value of 4.7uH.

2.8 DIGITAL POWER AND SYSTEM CONTROL INTERFACE

Signal Name	Pin No.	Type	Description
VCCO	7, 39	P	**3.3V I/O Power Supply.**
VCCK	4, 10, 40	P	**1.2V Core Power Supply.**
GND	E-PAD	P	**Ground.**
RST#	38	DI	**System Global Reset Input.** Schmitt trigger input pin. Active-low to reset the entire chip. An external RC should be connected to this pin.
TME	1	DI	**MP Test Mode Enable.** Schmitt trigger input pin. This pin is reserved for IC mass production testing. Keep this pin to logic “0” in normal operation.
MODE[1:0]	42, 46	DIL	**Chip Operation Mode Selection.** Value MODE[1:0] = 2’b01 is recommended in normal operation. For the others, they are using in IC mass production testing.
GPIO[0]	2	DIOH	**Serial Flash (SO)** After power on status detecting, this pin becomes Data Output of serial flash. This pin is by default set to input.
GPIO[1]	3	DIOH	**Serial Flash (SCK)** This pin is Serial Flash Data Clock (SCK) of serial flash. This pin is by default set to output.
GPIO[2]	5	DIOH	**Serial Flash(SI)** Serial Flash Data Input (SI) of serial flash. This pin is by default set to output.
GPIO[3]	6	DIOH	**Serial Flash(CE0#**) This pin functions as Chip Enable (CE0#) of Serial Flash
GPIO[4]	8	DIOH	**GPIO[4]** Can be configured by customer firmware.
GPIO[5]	9	DIOH	**GPIO[5]** Can be configured by customer firmware.
GPIO[6]	11	DIOH	**GPIO[6]** Can be configured by customer firmware.
GPIO[7]	41	DIOH	**GPIO[7]** Can be configured by customer firmware.
UAO/GPIO[8]	37	DIOH	**8051 UART interface/GPIO[8]** Can be configured by customer firmware.
UAI/GPIO[9]	48	DIOH	**8051 UART interface/GPIO[9]** Can be configured by customer firmware.
NC	26, 47	N/A	**Non Connect** Don’t Care on the connectivity

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

LED Indicator

By default, GPIO[4] is used as HDD access indicator. If user has different application for LED function, please contact JMicron's AE before PCB layout.

GPIO initial value

All GPIOs are set as input mode and their internal pull-up function is enabled during reset. After reset, the firmware code programs all of GPIOs as input mode, and then the initial values of GPIOs are read and stored in the system RAM for future usage.

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

3. External SPI Flash

3.1 EXTERNAL FLASH PROM/EPROM

JMS578 supports standard SPI mode only.

Vendor Name	Model Name	Comment
PMC	Pm25LV512 Pm25LV010 Pm25LV020 25LD512 CE1007 25LD512 CE0953 25LV010 AE1008 25LD010 CE1001 25LD512 AE093	
Winbond	W25X10 W25X20BLSNIG 25X10AVNIG 25X10BVNIG W25X10BLSNIG W25X40BLSNIG W25X05CLSNIG W25X10CLSNIG W25X20CLSNIG 25X40CLNIG 25Q80BLNIG 25Q16CVSIG 25X40CLVIG	
PFLASH	PM25LD020-SCE PM25LD040 PM25LD512C2-SCER	
Sanyo	LE25FU206AMB	
MXIC	MX25L5121E MX25L512E 25L512 CM1 25L512 MC 25L2005 MC 25L4005 AMC 25L1605 DM2I 25L8005 MC	

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

	KH25L5121E	
GigaDevice	25Q10T 25Q20T 25Q40T 25D05BT	
EON	F10-100 GIP F40-100 GCP F16-100 HIP F80-100 HCP Q64-104 HIP	

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

4. Clock & Reset

4.1 Crystal input

Parameter	Symbol	Min	Typical	Max	Unit
Crystal start up time v.s AVDDL	$T_{Crystal}$			150	mS
Crystal Frequency	f_{clk}		30		MHz
Long term stability (Crystal Only)	$\Delta f_{MAX_Crystal}$	-30		30	ppm
Long term stability (On Board)	$\Delta f_{MAX_OnBoard}$	-150		150	ppm
Equivalent Series Resistance	**ESR**			55	OHM
Drive Level	**DL**		50		uW

4.2 Reset input

All functions will be initialized by reset except the Analog Power-On Reset Circuit depending on the Power on-off.

The reset input pin is the Schmitt trigger input pin. VT+ Schmitt Trigger Low to High Threshold Point is 1.31V and VT- Schmitt Trigger High to Low Threshold Point is 0.96V.

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

5. Electrical Characteristics

5.1 Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Digital 3.3V power supply	$VCCO_{(ABS)}$	-0.3	3.6	V
Digital 1.2V power supply	$VCCK_{(ABS)}$	-0.3	1.32	V
Analog 1.2V power supply	$AVDDL_{(ABS)}$	-0.3	1.32	V
Digital I/O input voltage	$V_{I(D)}$	-0.3	3.6	V
USB VBUS power supply	VBUS	4.0	5.5	V
Storage Temperature	$T_{STORAGE}$	-40	150	^oC

5.2 Recommended Power Supply Operation Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	3.0	3.3	3.6	V
Digital 1.2V power supply	VCCK	1.08	1.2	1.32	V
Analog 1.2V power supply	AVDDL	1.08	1.2	1.32	V
Digital I/O input voltage	$V_{I(D)}$	0	3.3	3.6	V
Ambient operation temperature	T_A	0		70	^oC
Case operation temperature	T_C	0		90	^oC
Junction Temperature	T_J			125	^oC

5.3 Recommended External Clock Source Conditions

Parameter	Symbol	Min	Typical	Max	Unit
External reference clock			30		MHz
Clock Duty Cycle		45	50	55	%

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

5.4 Power Supply DC Characteristics

5.4.1 Power On (No USB Connected)

USB2.0 PHY, USB3.0 PHY, SATA PHY will be OFF

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.01	0.1	0.3	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	22	26.5	35	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	20	22	30	mA

5.4.2 USB2.0 to SATA mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	50	55	65	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	110	117	130	mA

5.4.3 USB3.0 to SATA mode

@U0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	75	82	90	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	160	175	185	mA

@U3 state (suspend @S4)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	1	2	4	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	2	3	6	mA

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

@U1/U2 state (No pending commands, SATA OFF, USB2 OFF)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.3	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	19	24	29	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	15	20	25	mA

5.5 I/O DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input low voltage	V_{IL}			0.7	V
Input high voltage	V_{IH}	1.5			V
Output low voltage	V_{OL}			0.3	V
Output high voltage	V_{OH}	1.9			V
Output Current	I_O		10	12	mA

5.6 VBus Detector

There are two parts for VBUS de-bounce. One is hysteresis and the other one is logic glitch filter.

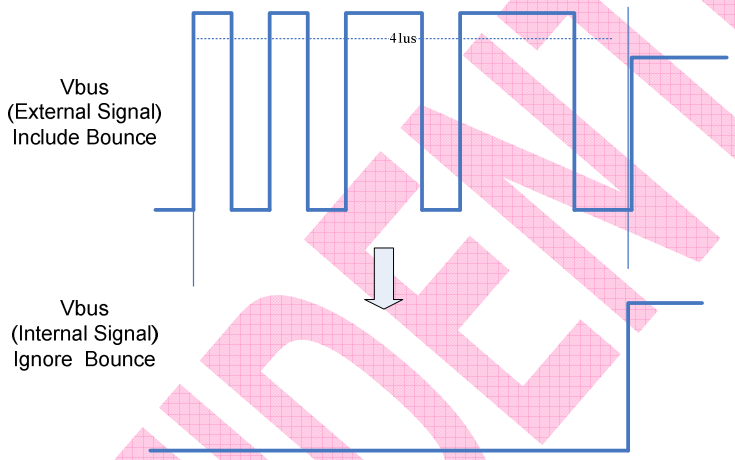
Hysteresis: switching threshold is 2.45V for high to low
switching threshold is 3.08V for low to high

CONFIDENTIAL

© JMicron 2014. All rights reserved.

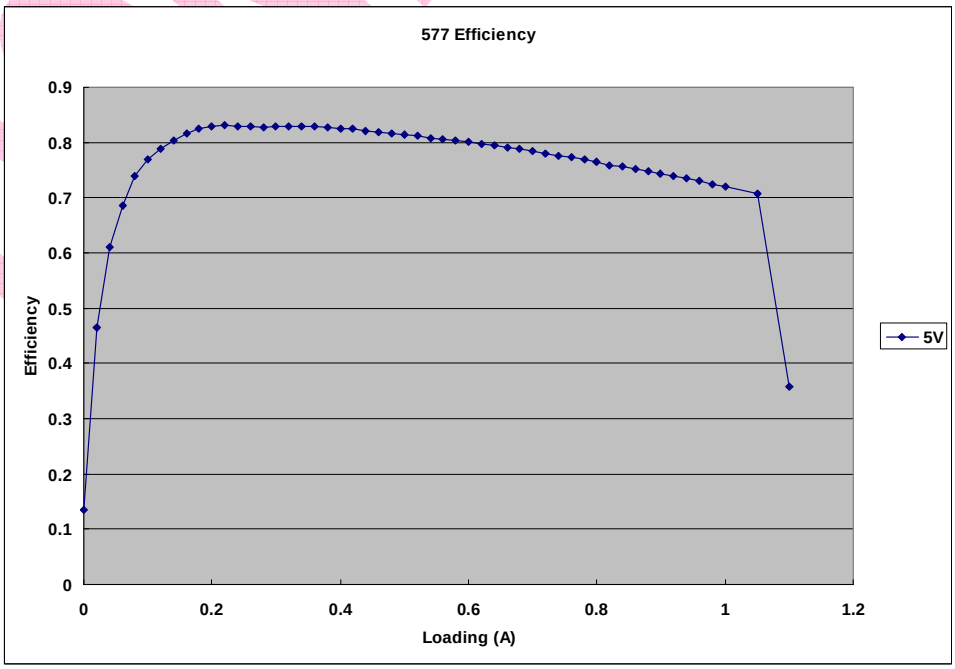
Copying prohibited.

And a 41us logical glitch filter is also implemented for VBUS de-bounce. If the logic high level is maintained for more than 41 us, the period will be treated as a HIGH period. Otherwise, the period will be LOW. The sample rate of VBUS is 100MH and checked status per 12 ms.



5.7 Switching Power efficiency (VREG_IN)

Efficiency = $Vout \times Iout / Vin \times Iin$ *, Vin = 5V, Vout = 1.2V*



© JMicron 2014. All rights reserved.

Copying prohibited.

5.8 Internal Linear Regulator

Parameter	Symbol	Min	Typical	Max	Unit
Input Voltage Range	V_{IN_LINEAR}	4	5	5.5	V
Output Voltage Range	V_{OUT_LINEAR}	3.10	3.3	3.45	V
Max Output Current	I_{MAX}	-	-	100	mA

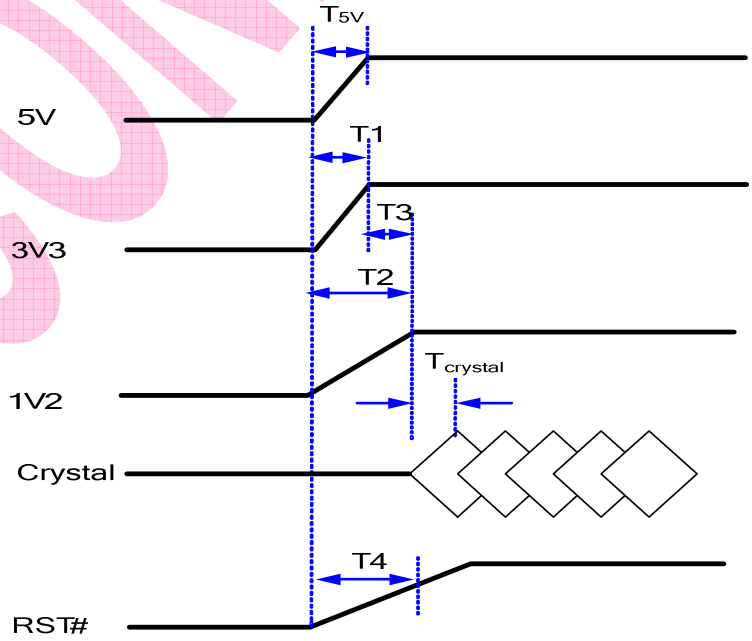
5.9 Power Ripple

Parameter	Symbol	Condition	Min	Typical	Max	Unit
5V Power Supply [1]	P_{5V}	Operate @ USB3.0	-	80	150	mV
3.3V Power Supply [2]	P_{3V3}	Operate @ USB3.0	-	80	150	mV
1.2V Power Supply [3]	P_{1V2}	Operate @ USB3.0	-	80	100	mV

Note: 1. Test point near Vbus capacitor.
2. Test point at LDO output capacitor.
3. Test point at AVDDL bypass capacitor.

5.10 Power-On Sequence

The Power-On sequence rules are defined in this section. Designers should follow all the rules for external power designs. Detailed explanations are listed as below.



T_{5V}: Rise time for 5V power rail from 10% to 90%

T1: Rise time for 3V3 power rail from 10% to 90%

© JMicron 2014. All rights reserved.

Copying prohibited.

T2: Rise time for 1V2 power rail from 10% to 90%

T3: Time interval between 3.3V power and 1.2V Power

T4: Rise time for RST# signal from 0.0V to 2.2V

$T_{Crystal:}$ Time interval between 1.2V and 90% clock swing

Note: Clock must meet 30MHz +/-30ppm in the mean time

The recommended power sequence and timing requirements are listed as below.

Time	Minimum	Maximum
T_{5V}	-	20 ms
T1	0.0 ms	10 ms
T2	0.0 ms	10 ms
T3	-10 ms	10 ms
T4	100 ms	500 ms
Tcrystal	-	150.0 ms

The RESET timing constrain is based on the external RC reset circuits. In order to control the charge and discharge time for RC circuits, minimum and maximum requirements are listed. If designers apply timing control chip to control the reset signal, the only requirement will be minimum value. In other words, the maximum value can be skipped without problems.

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

6. Internal Switch Regulator

Input Voltage Range: 2.25V ~ 5.50V
Output Voltage Range: 1.05V ~ 1.32V (programmable)
Output Voltage Accuracy : I_{LOAD}= 700 mA, V_{OUT}±10%
Max. Output Current : 700 mA
Over-Current Protection (OCP): Yes (1,500mA)
Input Capacitor: 10uF
Output Capacitor: 10uF ~ 20uF
Output Inductor: 4.7uH
Start-up Time : < 500us
Thermal Shutdown: No
Faster Shutdown: No

6.1 PCB layout guidelines :

1. Route high speed switching node LXO away from sensitive analog area (as crystal, REXT … etc)
2. Connect input/output capacitors to power and ground plane and put input/output capacitors close to IC and keep the high-current paths as short and wide as possible.

CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.

7. Performance Benchmark

7.1 Platform Configuration

Main Board	ASUS P8Z77 V PRO
CPU	Intel Core i3 2120 3.30GHz
RAM	Kingston DDR3-1333 2GB
BIOS version	v2104
OS	Windows 7 Ultimate x64 Windows 8.1 Enterprise x64
Host	Intel USB2 Host Intel USB3 Host

7.2 HDD List

SSD: Samsung 840 PRO 256GB

7.3 Test Tool

Crystal Disk Mark 3.02f
ATTO Disk Benchmark 2.47

CONFIDENTIAL

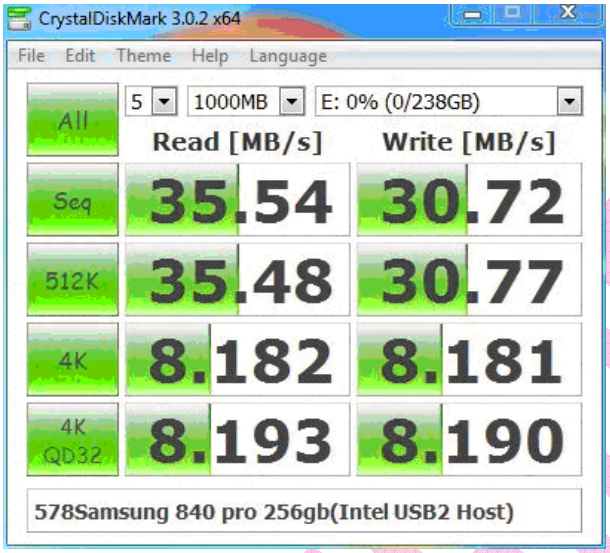
© JMicron 2014. All rights reserved.

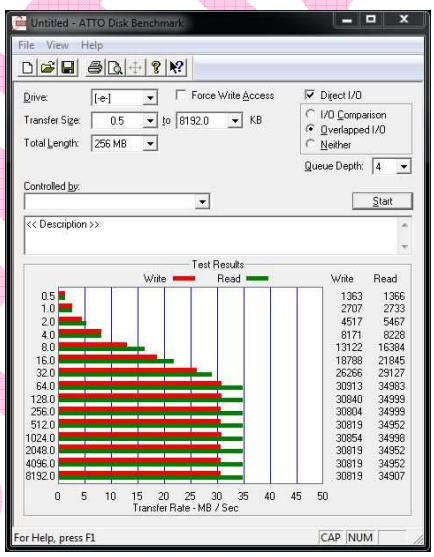
Copying prohibited.

7.4 JMS578 Performance

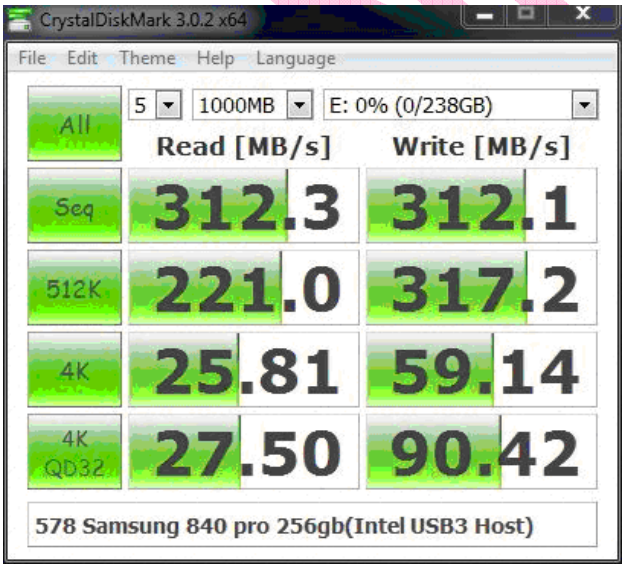
7.4.1 Win 7

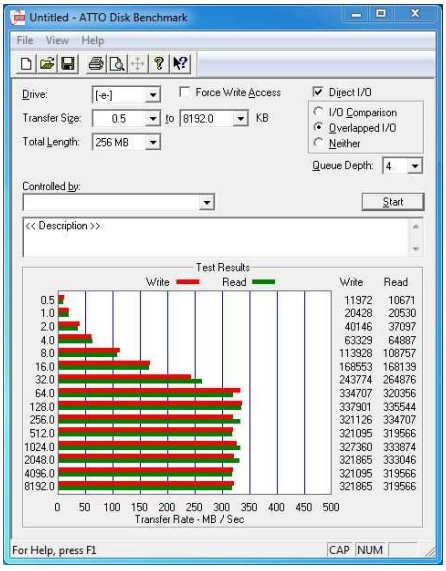
USB2.0 Performance for Win7





USB3.0 Performance for Win7





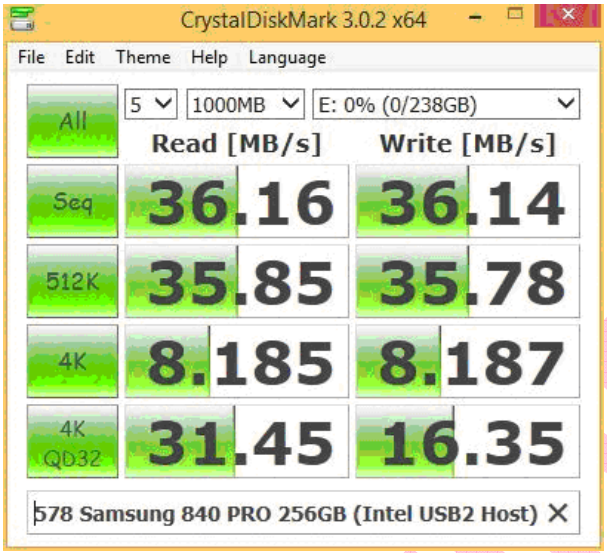
OFFICIAL

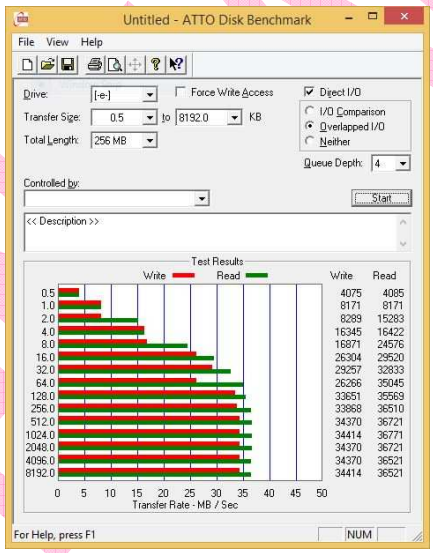
© JMicron 2014. All rights reserved.

Copying prohibited.

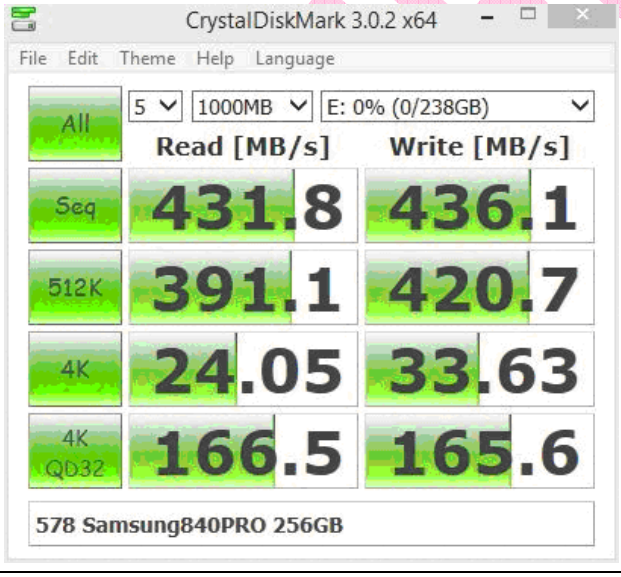
7.4.2 Win 8.1

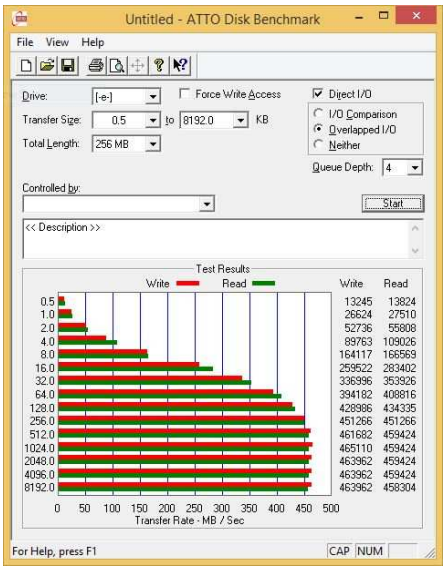
USB2.0 Performance for Win8.1





USB3.0 Performance for Win8.1



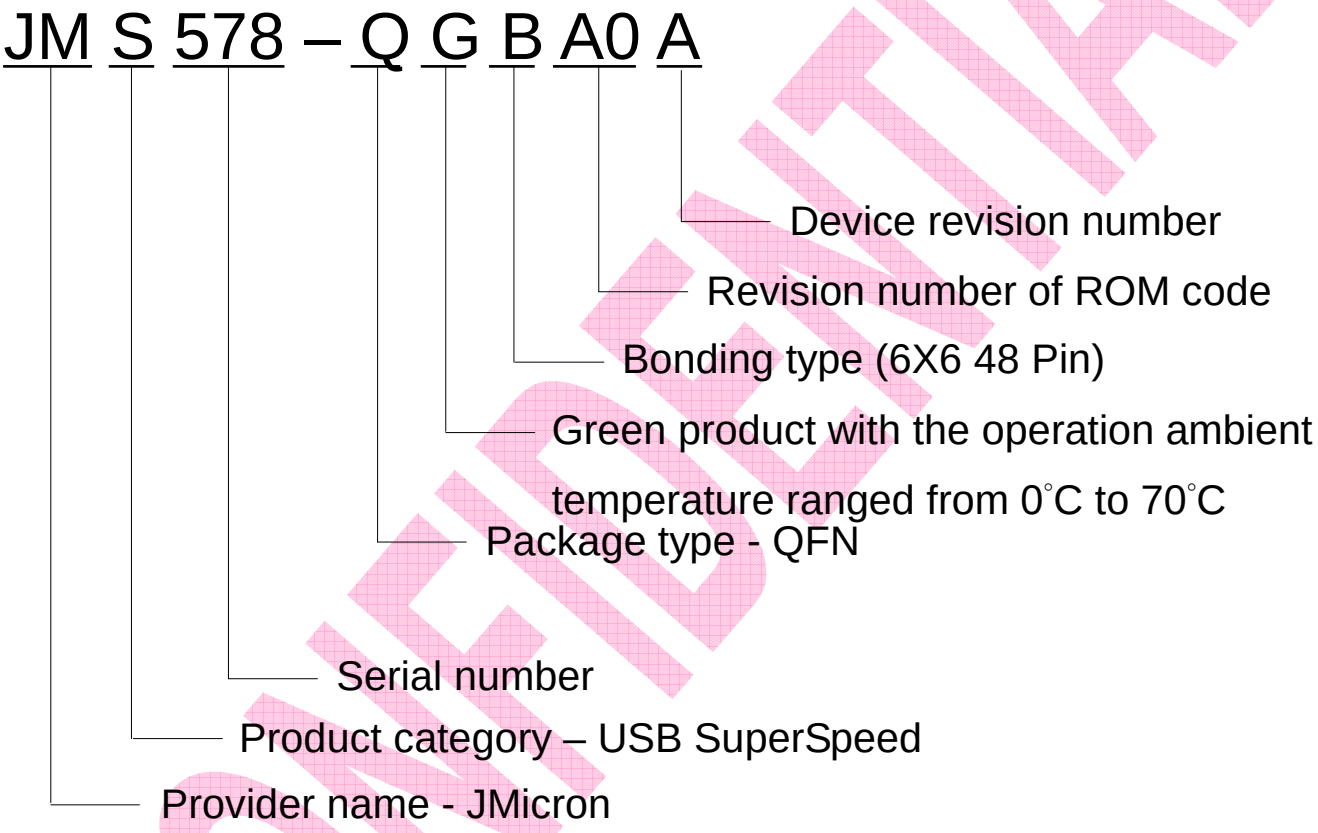


© JMicron 2014. All rights reserved.

Copying prohibited.

8. Product Naming

QFN48 6X6 mm^2



CONFIDENTIAL

© JMicron 2014. All rights reserved.

Copying prohibited.